WHAT IS CLAIMED IS:

1. A method of forming a bottom oxide layer in a trench structure, the method comprising:

providing a semiconductor substrate;

forming a silicon nitride layer on the semiconductor substrate;

forming a first oxide layer on the silicon nitride layer;

forming a trench structure in the semiconductor substrate;

forming a second oxide layer on a bottom and sidewalls of the trench and on a surface of the first oxide layer;

removing the first oxide layer and the second oxide layer on the surface of the silicon nitride layer; and

removing the second oxide layer on the sidewalls of the trench and a portion of the second oxide layer on the bottom of the trench.

2. The method according to claim 1 further comprises forming a pad oxide before forming the silicon nitride layer.

3. The method according to claim 1, wherein removing the first oxide layer and the second oxide layer on the surface of the silicon nitride layer is performed by a chemical mechanical polishing process.

4. The method according to claim 3, wherein the silicon nitride layer serves as a stop layer for the chemical mechanical polishing process.

5. The method according to claim 1, wherein forming a second oxide layer on the bottom and sidewalls of the trench and on the surface of the first oxide layer is performed by a Plasma Enhanced Tetra Ethyl Ortho Silicon (PE-TEOS) process.

6. The method according to claim 1, wherein the first oxide layer and the second oxide layer each comprise silicon oxide.

7. The method according to claim 1, wherein removing the second oxide layer on the sidewalls of the trench and portion of the second oxide layer on the bottom of the trench is performed by a wet etching process.

8. The method according to claim 7, wherein the wet etching process uses an etching solution comprising HF.

9. The method according to claim 7, wherein the wet etching process uses an etching solution, the etching solution being a Buffered Oxide Etch (BOE) solution comprising HF and NH_4F.

10. A method of manufacturing Diffused Metal-Oxide Semiconductor (DMOS) devices, the method comprising:

providing a semiconductor substrate;

forming a silicon nitride layer on the semiconductor substrate;

forming a first oxide layer on the silicon nitride layer;

forming a trench structure in the semiconductor substrate;

forming a second oxide layer on the bottom and sidewalls of the trench and on a surface of the first oxide layer;

removing the first oxide layer and the second oxide layer on the surface of the silicon nitride layer;

removing the second oxide layer on the sidewalls of the trench and a portion of the second oxide layer on the bottom of the trench;

forming a conductive layer over the silicon nitride layer on semiconductor substrate and the trench; and

removing the conductive layer on the silicon nitride layer.

11. The method according to claim 10, wherein the conductive layer comprises polysilicon.

12. The method according to claim 10 further comprises forming a pad oxide before forming the silicon nitride layer.

13. The method according to claim 10, wherein removing the first oxide layer and the second oxide layer on the surface of the silicon nitride layer is performed by a chemical mechanical polishing process.

14. The method according to claim 13, wherein the silicon nitride layer serves as a stop layer for the chemical mechanical polishing process.

15. The method according to claim 10, wherein forming a second oxide layer on the bottom and sidewalls of the trench and on the surface of the first oxide layer is performed by a Plasma Enhanced Tetra Ethyl Ortho Silicon (PE-TEOS) process.

16. The method according to claim 10, wherein the first oxide layer and the second oxide layer each comprise silicon oxide.

17. The method according to claim 10, wherein removing the second oxide layer on the sidewalls of the trench and portion of the second oxide layer on the bottom of the trench is performed with a wet etching process.

18. The method according to claim 17, wherein the wet etching process uses an etching solution comprising HF.

19. The method according to claim 17 wherein the wet etching process uses an etching solution, the etching solution being a Buffered Oxide Etch (BOE) solution comprising HF and NH_4F.

20. A method of forming a bottom oxide layer in a trench of a semiconductor substrate, the method comprising:

providing a semiconductor substrate including a trench disposed between islands having a first oxide layer formed thereon;

forming a second oxide layer over the first oxide layer of the islands and on a bottom and sidewalls of the trench;

removing the first oxide layer and the second oxide layer from the islands; and

removing the second oxide layer on the sidewalls of the trench and a portion of the second oxide layer on the bottom of the trench.

21. The method according to claim 20, wherein the second oxide layer is formed by a Plasma Enhanced Tetra Ethyl Ortho Silicon (PE-TEOS) process, and is thicker on the bottom of the trench than on the sidewalls of the trench.

22. The method according to claim 20, wherein the first oxide layer and the second oxide layer are removed from the islands by chemical mechanical polishing.

23. The method according to claim 20, wherein removing the second oxide layer on the sidewalls of the trench and a portion of the second oxide layer on the bottom of the trench is performed with a wet etching process.